AMENDMENTS TO THE CLAIMS

Please cancel claims 6, 12, 21, 22 and 24 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

a first circuit configured to generate a plurality of difference values by calculating an absolute difference between each pixel from a current block and a corresponding pixel from a reference block substantially simultaneously;

a second circuit configured to generate a plurality of sum values by adding said difference values; and

a third circuit configured to generate (i) a mode signal identifying a best mode among at least four partition modes, (ii) a motion signal conveying at least one motion vector associated with said best mode and (iii) a score signal conveying a score value associated with said best mode all in response to said sum values, wherein said third circuit comprises (i) an adder circuit configured to generate a plurality of first intermediate values from said sum values, (ii) a storage circuit configured to generate a plurality of second intermediate values from said first intermediate values as said current block is moved through a search window, (iii) a select circuit configured to generate (a) said mode signal, (b) said motion signal and (c) said score signal all from said second intermediate values, and (iv) a first bias circuit

configured to generate a cost value based on all of (a) a quantization parameter and (b) a motion vector magnitude and wherein said adder circuit is further configured to add said cost value to each of said first intermediate values.

2. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said first circuit comprises a plurality of processing elements each configured to generate one of said difference values.

3. (PREVIOUSLY PRESENTED) The apparatus according to claim 2, wherein said processing elements are logically configured as a two-dimensional array receiving said pixels from said current block and said reference block on a first side of said array and presenting said difference values on a second side of said array.

4. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said second circuit comprises a plurality of adder circuits each configured to generate one of said sum values substantially simultaneously by adding a unique combination of said difference values.

5. (CANCELED)

6. (CANCEL)

7. (CURRENTLY AMENDED) The apparatus according to claim 1 ~~6~~, wherein each of said first intermediate values corresponds to one of said partition modes of said current block.

8. (CANCELED)

9. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein each of said sum values corresponds to a smallest partition among said partition modes of said current block.

10. (CANCELED)

11. (CURRENTLY AMENDED) A method for motion estimation, comprising the steps of:

(A) generating a plurality of difference values by calculating an absolute difference between each pixel from a current block and a corresponding pixel from a reference block substantially simultaneously;

(B) generating a plurality of sum values by adding said difference values;

(C) generating a mode signal identifying a best mode among at least four partition modes in response to said sum values;

(D) generating a motion signal conveying at least one motion vector associated with said best mode in response to said sum values; [and]

(E) generating a score signal conveying a score value associated with said best mode in response to said sum values;

(F) generating a plurality of first intermediate values from said sum values, one of said intermediate values corresponding to each of said partition modes of said current block;

(G) generating a cost value based on all of (i) a quantization parameter and (ii) a motion vector magnitude; and

(H) adding said cost value to each of said first intermediate values.

12. (CANCEL)

13. (CURRENTLY AMENDED) The method according to claim 11 ~~12~~, further comprising the step of:

generating a plurality of minimum values by retaining a smallest of said sum values corresponding to each of said first intermediate values as said current block is moved through a search window.

14. (PREVIOUSLY PRESENTED) The method according to claim 13, further comprising the step of:

generating a plurality of second intermediate values by adding a plurality of bias values to said minimum values.

15. (PREVIOUSLY PRESENTED) The method according to claim 14, wherein step (D) further comprises the sub-step of:

generating said motion signal by determining a best of said second intermediate values.

16. (PREVIOUSLY PRESENTED) The method according to claim 11, further comprising the step of:

generating a first subset of a plurality of first intermediate values by adding a first group said difference values in a plurality of unique combinations.

17. (PREVIOUSLY PRESENTED) The method according to claim 16, wherein a second subset of said first intermediate values comprises a second group of said sum values.

18. (CANCELED)

19. (CANCELED)

20. (CURRENTLY AMENDED) A circuit comprising:

means for generating a plurality of difference values by calculating an absolute difference between each pixel from a current block and a corresponding pixel from a reference block substantially simultaneously;

means for generating a plurality of sum values by adding said difference values substantially simultaneously; and

means for generating (i) a mode signal identifying a best mode among at least four partition modes, (ii) a motion signal conveying at least one motion vector associated with said best mode and (iii) a score signal conveying a score value associated with said best mode all in response to said sum values, wherein said third circuit comprises (i) an adder circuit configured to generate a plurality of first intermediate values from said sum values, (ii) a storage circuit configured to generate a plurality of second intermediate values from said first intermediate values as said current block is moved through a search window, and (iii) a select circuit configured to generate (i) said mode signal, (ii) said motion signal and (iii) said score signal all from said second intermediate values, and (iv) a first bias circuit configured to generate a cost value based on all of (a) a quantization parameter and (b) a motion vector magnitude and wherein said adder circuit is further configured to add said cost value to each of said first intermediate values.

21. (CANCEL)

22. (CANCEL)

23. (PREVIOUSLY PRESENTED) The apparatus according to claim 22, wherein (i) said third circuit further comprises a second bias circuit configured to generate a plurality of bias values based on said quantization parameter and (ii) said second circuit is further configured to add each one of said bias values to a respective one of said second intermediate values.

24. (CANCEL)

25. (PREVIOUSLY PRESENTED) The method according to claim 14, wherein said bias values are generated based on a quantization parameter.

26. (NEW) An apparatus comprising:

a first circuit configured to generate a plurality of difference values by calculating an absolute difference between each pixel from a current block and a corresponding pixel from a reference block substantially simultaneously;

a second circuit configured to generate a plurality of sum values by adding said difference values; and

a third circuit configured to generate (i) a mode signal identifying a best mode among at least four partition modes, (ii) a motion signal conveying at least one motion vector associated with said best mode and (iii) a score signal conveying a score value associated with said best mode all in response to said sum values, wherein said third circuit comprises (i) an adder circuit configured to generate a plurality of first intermediate values from said sum values, (ii) a storage circuit configured to generate a plurality of second intermediate values from said first intermediate values as said current block is moved through a search window, and (iii) a select circuit configured to generate (a) said mode signal, (b) said motion signal and (c) said score signal all from said second intermediate values and wherein said second circuit is further configured to generate (i) a plurality of minimum values by retaining a smallest of said sum values corresponding to each of said first intermediate values and (ii) generate said second intermediate values by adding a plurality of bias values to said minimum values.